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| **Modulus Project Status (11/13/2015 - 05:13:49)** | | | |
| **Project File:** | Co\_Design.xise | **Parser Errors:** | No Errors |
| **Module Name:** | Modulus | **Implementation State:** | Placed and Routed |
| **Target Device:** | xa7z010-1Iclg400 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.4 | * **Warnings:** | [88 Warnings (10 new)](D://embedded_system_design/Co_Design/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://embedded_system_design/Co_Design/Modulus.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://embedded_system_design/Co_Design/Modulus.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://embedded_system_design/Co_Design/Modulus_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://embedded_system_design/Co_Design/Modulus.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 70 | 35,200 | 1% |  | |
| Number used as Flip Flops | 70 |  |  |  | |
| Number used as Latches | 0 |  |  |  | |
| Number used as Latch-thrus | 0 |  |  |  | |
| Number used as AND/OR logics | 0 |  |  |  | |
| Number of Slice LUTs | 154 | 17,600 | 1% |  | |
| Number used as logic | 154 | 17,600 | 1% |  | |
| Number using O6 output only | 147 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 7 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 6,000 | 0% |  | |
| Number used exclusively as route-thrus | 0 |  |  |  | |
| Number of occupied Slices | 82 | 4,400 | 1% |  | |
| Number of LUT Flip Flop pairs used | 189 |  |  |  | |
| Number with an unused Flip Flop | 122 | 189 | 64% |  | |
| Number with an unused LUT | 35 | 189 | 18% |  | |
| Number of fully used LUT-FF pairs | 32 | 189 | 16% |  | |
| Number of unique control sets | 3 |  |  |  | |
| Number of slice register sites lost         to control set restrictions | 2 | 35,200 | 1% |  | |
| Number of bonded [IOBs](D://embedded_system_design/Co_Design/Modulus_map.xrpt?&DataKey=IOBProperties) | 74 | 100 | 74% |  | |
| Number of RAMB36E1/FIFO36E1s | 0 | 60 | 0% |  | |
| Number of RAMB18E1/FIFO18E1s | 0 | 120 | 0% |  | |
| Number of BUFG/BUFGCTRLs | 1 | 32 | 3% |  | |
| Number used as BUFGs | 1 |  |  |  | |
| Number used as BUFGCTRLs | 0 |  |  |  | |
| Number of IDELAYE2/IDELAYE2\_FINEDELAYs | 0 | 100 | 0% |  | |
| Number of ILOGICE2/ILOGICE3/ISERDESE2s | 0 | 100 | 0% |  | |
| Number of ODELAYE2/ODELAYE2\_FINEDELAYs | 0 |  |  |  | |
| Number of OLOGICE2/OLOGICE3/OSERDESE2s | 0 | 100 | 0% |  | |
| Number of PHASER\_IN/PHASER\_IN\_PHYs | 0 | 8 | 0% |  | |
| Number of PHASER\_OUT/PHASER\_OUT\_PHYs | 0 | 8 | 0% |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHCEs | 0 | 48 | 0% |  | |
| Number of BUFRs | 0 | 8 | 0% |  | |
| Number of CAPTUREs | 0 | 1 | 0% |  | |
| Number of DNA\_PORTs | 0 | 1 | 0% |  | |
| Number of DSP48E1s | 0 | 80 | 0% |  | |
| Number of EFUSE\_USRs | 0 | 1 | 0% |  | |
| Number of FRAME\_ECCs | 0 | 1 | 0% |  | |
| Number of ICAPs | 0 | 2 | 0% |  | |
| Number of IDELAYCTRLs | 0 | 2 | 0% |  | |
| Number of IN\_FIFOs | 0 | 8 | 0% |  | |
| Number of MMCME2\_ADVs | 0 | 2 | 0% |  | |
| Number of OUT\_FIFOs | 0 | 8 | 0% |  | |
| Number of PHASER\_REFs | 0 | 2 | 0% |  | |
| Number of PHY\_CONTROLs | 0 | 2 | 0% |  | |
| Number of PLLE2\_ADVs | 0 | 2 | 0% |  | |
| Number of PS7s | 0 | 1 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of XADCs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 1.77 |  |  |  | |

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| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://embedded_system_design/Co_Design/Modulus_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://embedded_system_design/Co_Design/Modulus.unroutes) | **Clock Data:** | [Clock Report](D://embedded_system_design/Co_Design/Modulus_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** | [All Constraints Met](D://embedded_system_design/Co_Design/Modulus.ptwx?&DataKey=ConstraintsData) |  |  | |

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| **Detailed Reports** | | | | | | [**[-]**](?&ExpandedTable=DetailedReports) |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| [Synthesis Report](D://embedded_system_design/Co_Design/Modulus.syr) | Current | Fri 13. Nov 05:01:52 2015 | 0 | [12 Warnings (10 new)](D://embedded_system_design/Co_Design/_xmsgs/xst.xmsgs?&DataKey=Warning) | [1 Info (1 new)](D://embedded_system_design/Co_Design/_xmsgs/xst.xmsgs?&DataKey=Info) | |
| [Translation Report](D://embedded_system_design/Co_Design/Modulus.bld) | Current | Fri 13. Nov 05:04:50 2015 | 0 | 0 | 0 | |
| [Map Report](D://embedded_system_design/Co_Design/Modulus_map.mrp) | Current | Fri 13. Nov 05:08:20 2015 | 0 | [76 Warnings (0 new)](D://embedded_system_design/Co_Design/_xmsgs/map.xmsgs?&DataKey=Warning) | [7 Infos (2 new)](D://embedded_system_design/Co_Design/_xmsgs/map.xmsgs?&DataKey=Info) | |
| [Place and Route Report](D://embedded_system_design/Co_Design/Modulus.par) | Current | Fri 13. Nov 05:11:32 2015 | 0 | 0 | [2 Infos (0 new)](D://embedded_system_design/Co_Design/_xmsgs/par.xmsgs?&DataKey=Info) | |
| Power Report |  |  |  |  |  | |
| [Post-PAR Static Timing Report](D://embedded_system_design/Co_Design/Modulus.twr) | Current | Fri 13. Nov 05:13:34 2015 | 0 | 0 | [4 Infos (0 new)](D://embedded_system_design/Co_Design/_xmsgs/trce.xmsgs?&DataKey=Info) | |
| Bitgen Report |  |  |  |  |  | |

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| **Secondary Reports** | | | [**[-]**](?&ExpandedTable=SecondaryReports) |
| **Report Name** | **Status** | **Generated** | |
| [ISIM Simulator Log](D://embedded_system_design/Co_Design/isim.log) | Out of Date | Thu 12. Nov 12:58:12 2015 | |

**Date Generated:** 11/13/2015 - 05:21:09